CLAIMS:

What is claimed is:

1. A semiconductor capacitor comprising:

a first conductive section having a first outer plate connected to a first inner plate; and

a second conductive section having a second outer plate connected to a second inner plate, wherein the second inner plate is located within a first hole in the first outer plate and the first inner plate is located within a second hole in the second outer plate such that a first distance is present between the second inner plate and the first outer plate and a second distance is present between the first inner plate and the second outer plate.

2. The semiconductor capacitor of claim 1, wherein the semiconductor capacitor is a complimentary metal-oxide semiconductor capacitor.

3. The semiconductor capacitor of claim 1, wherein the first outer plate and the second outer plate have a rectangular shape.

4. The semiconductor capacitor of claim 1, wherein the first distance is equal to the second distance.

5. The semiconductor capacitor of claim 1, wherein the first distance is about 0.2 μm and the second distance is about 0.2 μm.

6. The semiconductor capacitor of claim 1, wherein the first section and the second section have a thickness of about 0.25 μm to about 0.45 μm.

7. The semiconductor capacitor of claim 1 further comprising:

a third conductive section having an third outer plate connected to a third inner plate; and

a fourth conductive section having a fourth outer plate connected to a fourth inner plate, wherein the fourth inner plate is located within a third hole in the third outer plate and the third inner plate is located within a fourth hole in the fourth outer plate such that a third distance is present between the fourth inner plate and the third outer plate and a fourth distance is present between the third inner plate and the fourth outer plate and wherein the third conductive section and the fourth conductive section are located below the first conductive section and the second conductive section.

8. The semiconductor capacitor of claim 1, wherein the third outer plate is located below the first outer plate, fourth outer plate is located below the second outer plate, the third inner plate is located below the first inner plate, and the fourth inner plate is located below the second inner plate.

9. The semiconductor capacitor of claim 1, the first conductive section is connected to a third conductive section by a first set of via connections and wherein the second conductive section is connected to the fourth conductive section by a second set of via connections.

10. The semiconductor capacitor of claim 9, wherein first conductive section is spaced apart of the third section by about 0.2 μm and the second conductive section is spaced apart from the fourth conductive section by about 0.2 μm.

11. The semiconductor capacitor of claim 1, wherein the first conductive section and the second conductive section are formed from a metal layer.

12. The semiconductor capacitor of claim 1, wherein the first outer plate is connected to the first inner plate by a first metal line and wherein the second outer plate is connected to the second inner plate by a second metal line.

13. A method for fabricating a semiconductor capacitor, the method comprising:

forming a bottom metal layer on an insulator;

etching the bottom metal layer to form a first bottom conductive section having an first outer plate and a first inner plate and a second bottom conductive section having a second outer plate and a second inner plate, wherein the second inner plate is located within a first hole in the first outer plate and the first inner plate is located within a second hole in the second outer plate;

forming a first dielectric layer over the first bottom conductive section plate and the second bottom conductive section;

forming a first set of interconnects through the first dielectric layer, wherein the first set of interconnects are in contact with the first bottom conductive section and the second bottom conductive section;

forming a top metal layer in contact with the first set of interconnects;

etching the top metal layer to form a first top conductive section having an first outer plate and a first inner plate and a second top conductive section having a second outer plate and a second inner plate, wherein the second inner plate is located within a first hole in the first outer plate and the first inner plate is located within a second hole in the second outer plate;

forming a second dielectric layer on the first top conductive section and the second top conductive section;

forming a second set of via interconnects through the second dielectric layer, wherein the second set of interconnects are in contact with the first top conductive section and the second top conductive section;

forming a first metal line from a first via interconnect in the second set of via interconnects to a second via interconnect in the second set of via interconnects to connect the first outer plate in the first top conductive section to the first inner plate in the first top conductive section; and

forming a second metal line from a third via interconnect in the second set of via interconnects to a fourth via interconnect in the second set of via interconnects to connect the second outer plate in the first top conductive section to the second inner plate in the first top conductive section.

14. The method of claim 13, wherein the first dielectric layer and the second dielectric layer are formed from SiO_2.

15. The method of claim 13, wherein the bottom metal layer is formed using copper.